Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application.

Listing of Claims

1. (canceled)

2. (canceled)

3. (canceled)

4. (canceled)

5. (canceled)

6. (canceled)

7. (canceled)

8. (canceled)

9. (canceled)

10. (previously presented) An egress selection switch, comprising:

a plurality of ingress ports for transmitting a plurality of ingress data grains;

said plurality of egress ports forming at least two egress port groups;

a timeslot counter for identifying a particular timeslot number for each ingress data grain of said plurality of ingress data grains; and

a plurality of data disable blocks for fanout of ingress data grains to at least one of said plurality of egress ports, each data disable block of said plurality of data disable blocks having:

- a data disable control memory; and

- a plurality of flip flops being coupled to said data disable control memory, each data storage device of said plurality of data storage devices propagating a particular ingress data grain to a particular egress port group and enabling propagation of said particular ingress data grain based on information stored in said data disable control memory, wherein a particular flip flop of said plurality of flip flops toggles said particular ingress data grain as said particular flip flop is logically enabled based on information stored in said data disable control memory;

wherein said data disable control memory is connected to said plurality of data storage devices and is coupled to a microprocessor interface for updating said information stored in said data disable control memory; and

wherein said time slot counter is coupled to said data disable control memory.

11. (original) The egress selection switch as in claim 10, wherein said information stored in said data disable control memory is data bit information.

12. (canceled)

13. (canceled)

14. (canceled)

15. (previously presented) The egress selection switch as in claim 10, wherein each of said plurality of flip flops is a D type flip flop.

16. (previously presented) The egress selection switch as in claim 10, wherein each of said plurality of flip flops is connected to a clock gating circuit.

17. (original) The egress selection switch as in claim 10, further including a plurality of grain select blocks for selecting and storing said plurality of ingress data grains received from said plurality of data disable blocks, and a system for outputting a pre-defined egress data grain to one of said plurality of egress ports, wherein said plurality of grain select blocks are coupled to said plurality of data disable blocks.

18. (canceled)

19. (canceled)

20. (canceled)

21. (previously presented) A method for improving efficiency of a data switch, said data switch propagating transmission of ingress data to at least one egress port in a predefined interval of time from an ingress side of said switch to an egress side of said switch, said method comprising steps:

a) grouping a plurality of egress ports into at least two egress port groups;

b) generating signals containing a predefined data selection for propagation, from said egress side to said ingress side, through a data fanout tree;

c) disabling propagation of said ingress data to at least one egress port group of said at least two egress port groups based on said predefined data selection;

d) overwriting by a constant value half the bits asserted by said ingress data disabled in step c);

e) defining egress data based on said predefined data selection of said ingress data by at least one egress port group being enabled for propagation of said ingress data; and

f) storing said egress data and said ingress data for output to said corresponding egress port.

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~~23.~~ (previously presented) A method for improving efficiency of a data switch, said data switch propagating transmission of ingress data to at least one egress port in a predefined interval of time from an ingress side of said switch to an egress side of said switch, said method comprising steps:

a) grouping a plurality of egress ports into at least two egress port groups;

b) generating signals containing a predefined data selection for propagation, from said egress side to said ingress side, through a data fanout tree, said fanout tree having at least one pair of sub-trees;

c) disabling propagation of said ingress data to at least one egress port group of said at least two egress port groups based on said predefined data selection ;

d) overwriting by a first constant value said ingress data derived from an enable signal through a first of said at least one pair of sub-trees and by a second constant value said ingress data derived from an enable signal through a second of said at least one pair of sub-trees, such that said first constant value and said constant value are complementary and said first constant value and said second constant value form a different complementary pair of constants for each pair of sub-trees;

e) defining egress data based on said predefined data selection of said ingress data by at least one egress port group being enabled for propagation of said ingress data; and

f) storing said egress data and said ingress data for output to said corresponding egress port.

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24. (canceled)

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25. (previously presented) An egress selection switch, comprising:

a plurality of grain select blocks for selecting and storing a plurality of ingress data grains, each grain select block having:

- a connection memory having memory contents defining an egress data grain at a corresponding grain select block, said egress data grain being defined by a pre-selected ingress port and a pre-selected timeslot of said plurality of ingress data grains;
- a multiplexer for selecting a particular ingress data grain through fanout based on said pre-selected ingress port and said pre-selected timeslot in said connection memory;
- a data storage device for storing output received from said multiplexer; and
- means for outputting said egress data grain from said data storage device to said plurality of egress ports;

wherein said connection memory having decode logic to generate a signal from said each grain select block for selectively enabling and disabling fanout of said plurality of ingress data grains; and

a main timeslot counter for identifying a particular timeslot number for each ingress data grain of said plurality of ingress data grains, and a lookahead timeslot counter provided to

compensate for delay occurring in said decode logic, wherein said lookahead timeslot counter runs ahead of said main timeslot counter.

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26. (previously presented) A system for improving power efficiency of a memory switch, said memory switch enabling propagation of data, through said memory switch, from a source to a plurality of destinations, said system comprising:

at least one grain select block for selecting and storing specific data, said specific data being propagated to a subset of destinations within said plurality of destinations, each grain select block containing fanout information for propagating said specific data to said subset of destinations through a fanout tree;

at least one data disable block for providing a data connection from said source to said at least one grain select block based on said fanout information, said at least one data disable block receiving said data from said source;

wherein said specific data is propagated over a pre-defined interval of time from said at least one data disable block to said at least one grain select block, and

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wherein said fanout information is generated as a signal propagating from a tail end of said fanout tree to a root end of said fanout tree to enable propagation of said specific data from said source.

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27. (original) The system as in claim 26, wherein said fanout tree includes logical OR trees and logical AND trees, wherein said logical OR trees propagate said fanout information to said at least one grain select block and said logical AND trees disables a portion of said fanout tree by one propagating said specific data to said subset of destinations.

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28. (previously presented) A method of reducing power consumption in a time division multiplexing (TDM) egress selection memory switch having an ingress side with a plurality of ingress ports, an egress side with a plurality of egress ports, and fanout circuitry connecting the ingress side and the egress side, the method comprising:

grouping the plurality of egress ports into at least two egress port groups;

selecting and storing a given ingress grain for eventual output through the fanout circuitry; and

reducing average power consumption of the fanout circuitry by selectively propagating the ingress grain data to a selected egress port group, the selected egress port group having at least one egress port for which the given ingress grain is selected for output.

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29. (previously presented) The method of claim 28 wherein the step of reducing the average power consumption of the fanout circuitry further comprises:

upon receipt of the ingress grain data at the selected egress port group, further selectively propagating the ingress grain data for decoding to a selected egress register within the at least one egress port for which the given ingress grain is selected for output.

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30. (previously presented) The method of claim 29 wherein the further selective propagation for decoding to only the selected egress register is based on decoded connection memory settings.

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31. (previously presented) The method of claim 28 further comprising:

marking the given ingress grain as selected for output by any port within the selected egress port group.

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32. (previously presented) The method of claim 28 wherein the step of selectively propagating the ingress grain data to only a selected egress port group comprises disabling unselected grains, and further comprising:

selectively overwriting bits in the disabled grains in the fanout circuitry with a constant value having an equal number of high and low bits, the disabled grains being internal to the switch, in order to reduce a timeslot transition peak power spike amplitude.

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33. (previously presented) A system for reducing power consumption in a time division multiplexing (TDM) egress selection memory switch, the memory switch having an ingress side with a plurality of ingress ports, an egress side with a plurality of egress ports, and fanout circuitry connecting the ingress side and the egress side, the system comprising:

at least one power reduction block for reducing average power consumption of the fanout circuitry by selectively propagating a given ingress grain to only a group of egress ports which is a subset of the plurality of egress ports, the group of egress ports having at least one egress port for which the given ingress grain is selected for output; and

at least one grain select block for selecting and storing the given ingress grain for eventual output through the fanout circuitry, each grain select block including fanout information for propagating the ingress grain to the group of egress ports.

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34. (previously presented) A method of power leveling in a time division multiplexing (TDM) egress selection memory switch having an ingress side with a plurality of ingress ports, an egress side with a plurality of egress ports, and fanout circuitry connecting the ingress side and the egress side, the method comprising:

selecting and storing ingress grains for eventual output through the fanout circuitry;

identifying disabled grains that will not be propagated through the fanout circuitry since no selected egress port exists for a given timeslot; and

selectively overwriting bits in the disabled grains in the fanout circuitry with a constant value, the disabled grains being internal to the switch, in order to reduce a timeslot transition peak power spike amplitude.

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35. (new) The method of claim 34 wherein the constant value includes an equal number of logic 0 and logic 1 bits.

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36. (new) The method of claim 34 wherein selectively modifying bits in the disabled grains comprises:

selectively modifying disabled grains in a first egress port switching block with a first constant value; and

selectively modifying disabled grains in a second egress port switching block with a second constant value, the second constant value being a logical complement of the first constant value.

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37. (new) A system for power leveling in a time division multiplexing (TDM) egress selection memory switch, the memory switch having an ingress side with a plurality of ingress ports, an egress side with a plurality of egress ports, and fanout circuitry connecting the ingress side and the egress side, the system comprising:

at least one power leveling block for reducing a timeslot transition peak power spike amplitude of the fanout circuitry by selectively overwriting bits in disabled grains in the fanout circuitry with a constant value, the disabled grains being internal to the switch, the disabled

grains not being propagated through the fanout circuitry since no selected egress port exists for a given timeslot; and

at least one grain select block for selecting and storing the ingress grains for eventual output through the fanout circuitry, each grain select block including fanout information for propagating the ingress grain to the group of egress ports.